Docket No.: 50100-754

UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Stephen McROBERT
FOR: MATCH SIGNALS IN DATA SWITCHING SYSTEMS INCLUDING MULTIPLE SWITCHING DEVICES

Enclosed are:

- ☒ 12 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☐ Certified copy of _____
- ☒ 3 sheets of formal drawing.
- ☒ An assignment of the invention to Advanced Micro Devices, Inc. and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☐ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☒ Preliminary Amendment

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	15	-20	0	$18.00	$0.00
Independent Claims	2	-3	0	$78.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$690.00
				Total of Above Calculations	$690.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
				Total Fee	$730.00

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☒ Any patent application processing fees under 37 CFR 1.17.

☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

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Docket No.: 50100-754 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Stephen McROBERT	:	
Serial No.:	:	Group Art Unit:
Filed: June 15, 2000	:	Examiner:

For: MATCH SIGNALS IN DATA SWITCHING SYSTEMS INCLUDING MULTIPLE SWITCHING DEVICES

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE SPECIFICATION:

Page 1, after the title, please insert the following:

--Related Applications

This application claims priority from U.S. Provisional Patent Application No. 60/152,949, filed September 9, 1999, which is incorporated herein by reference.--

REMARKS

This application is being amended to insert the related application information. Entry of this preliminary amendment is respectfully requested.

Respectfully submitted,

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D223

MATCH SIGNALS IN DATA SWITCHING SYSTEMS INCLUDING MULTIPLE SWITCHING DEVICES

Field of the Invention

The present invention relates to data communications, and more particularly, to producing matching signals for interconnecting address tables of multiple switching devices in a packet switching system.

Background Art

A switch including multiple switching devices may be provided in a data communication network to enable data communication between multiple network stations connected to various ports of the switch. A logical connection may be created between receive ports and transmit ports of the switching devices to forward received frames to appropriate destinations. Based on frame headers including source and destination address information, a frame forwarding arrangement makes a frame forwarding decision about which, if any, ports the frames will be forwarded to.

To support frame forwarding operations, each switching device maintains an address table containing source and destination address information. Whenever, a switching device receives a frame, it reads the source address of the frame, and if this address is not found in the table, an address entry corresponding to the port from whence the frame came may be added to the table. The switching device also reads the destination address of the frame, and if this address can be matched to a particular port, the device will forward the frame to that port.

In a switching system using multiple switching devices, the destination address of a frame may be not found in the address table of a particular switching device that receives the frame. In this case, the device will "flood" the frame to all of its ports and to an expansion bus connecting various switching devices of the switching system. However, frame flooding is undesirable because it uses up the bandwidth of the system.

Therefore, it would be desirable to create a mechanism that enables a switching system to share address table information among switching devices.

Disclosure of the Invention

The invention offers a novel method of data packet switching in a data packet switching system having multiple switching devices. The method includes comparing destination address information of a received data packet with current address information maintained by one or more of the switching devices, and supplying a match signal to other switching devices when the destination address information matches the current address information. For example, the current address information may be stored in an address table of the switching device. The address table of the switching device may be preset to specific values by the intervention of someone such as a system administrator. During normal operation, the values in the address table will be updated via several different mechanisms. The value of an address table prior to an update is referred in this application as its current value.

The switching devices that received the match signal are informed that the host with the destination address that caused the match signal is not connected to one of their own media ports. The match signal sent to other switching devices in the system is unambiguously associated with the destination address that caused the match. Further, the match signal may uniquely identify the switching device that generates this signal. In response to the match signal, the current address information of the other switching devices in the system may be updated in accordance with the destination address information that caused the match signal, to enable the switching system to forward traffic with that destination address to the appropriate switching device.

The device that generates the match signals and forwards the associated frame to the other devices in the switching system should do so only on the first occasion on which it detects an exact address match. On all subsequent occasions it should neither forward the frame nor assert the match signals, because forwarding the frame wastes bandwidth on the expansion bus connecting the switching devices together.

Each device in the switching system will update its address tables on this first occasion, and will not need to be reminded.

The novel method of data switching in accordance with the present invention may be implemented in a data communication system comprising multiple switching devices for switching data packets, and an expansion bus for transferring the data

packets between the switching devices. Each switching device has an address processing block for comparing destination address information of a received data packet with current address information, and producing a match signal supplied to another switching device when the destination address information matches the current information.

The address processing block may be configured for producing a forwarding control signal for forwarding the received data packet to a destination associated with the destination address information. Also, the address processing block may be configured for comparing source address information of a received data packet with the current address information to update the current address information in accordance with the source address information if the source address information does not match the current address information.

Each switching device may comprise a match pin connected to the match pin of another switching device to transfer the match signal. Alternatively, the match signal may be transferred via the expansion bus as a prefix or suffix to the data packet that caused the match signal. The match signal may indicate that a match occurred and may identify switching device generated the match signal.

Various objects and features of the present invention will become more readily apparent to those skilled in the art from the following description of a specific embodiment thereof, especially when taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a block diagram of a packet switched network including a switch having multiple switching devices according to an embodiment of the present invention.

Figure 2 is a simplified block diagram illustrating one of the multiple switching devices shown in Figure 1.

Figure 3 is a block diagram illustrating another embodiment of the present invention.

Best Mode for Carrying out the Invention

Figure 1 is a block diagram of an exemplary system in which the present invention may be advantageously employed. The exemplary system 10 is a packet switched network, such as an Ethernet (IEEE 802.3) network. The packet switched network comprises a switch unit including multiple switching devices 12 that enable communication of data packets between network stations. Although Figure 1 shows that the switch unit includes three switching devices 12a, 12b and 12c, the present invention is applicable to switching systems including any number of switching devices 12.

The network 10 may include network stations having different configurations, for example 10 megabit per second (Mb/s) or 100 Mb/s network stations 14 (hereinafter 10/100 Mb/s) that send and receive data at a network data rate of 10 Mb/s or 100 Mb/s. Each switching device 12 includes multiple media access control (MAC) ports that transmit and receive data frames to and from 10/100 Mb/s physical layer (PHY) transceivers 16 via respective media independent interfaces (MII) 18 according to IEEE 802.3u protocol.

Each 10/100 Mb/s network station 14 sends and receives data frames to and from the corresponding switching device 12 via a media 20 and according to either half-duplex or full duplex Ethernet protocol. The Ethernet protocol ISO/IEC 8802-3 (ANSI/IEEE Std. 802.3, 1993 Ed.) defines a half-duplex media access mechanism that permits all stations 14 to access the network channel with equality.

The 10/100 Mb/s network stations 14 that operate in full duplex mode send and receive data frames according to the Ethernet standard IEEE 802.3u. The full-duplex environment provides a two-way, point-to-point communication link enabling simultaneous transmission and reception of data packets between each link partner, i.e., the 10/100 Mb/s network station 14 and the corresponding switch 12.

Each switching device 12 is coupled to 10/100 Mb/s physical layer (PHY) transceivers 16 configured for sending and receiving data frames to and from the corresponding switching device 12 across a corresponding media independent interface (MII) 18. A magnetic transformer 22 provides AC coupling between the PHY transceiver 16 and the corresponding network medium 20.

Each switching device 12 may also include an expansion port 24 for transferring data to and from other switching devices via an expansion bus 26

according to a prescribed protocol. For example, the expansion bus 26 may be implemented as a "daisy chain" high bandwidth expansion bus. The expansion port 24 may be implemented as a gigabit MAC port for sending and transmitting data frames via the high-bandwidth expansion bus 26 at a network speed of 1 Gb/s.

As discussed in more detail later, each switching device 12 contains an address table for storing address information of network stations. Whenever a switching device 12 receives a frame, it compares the source address (SA) information of the frame with the address information in the address table. If the SA information does not match any address entry in the address table, the switching device 12 creates a new entry corresponding to the SA information.

Also, the switching device 12 compares the destination address (DA) information of each received frame with the address information in the address table. If the switching device 12 determines that the DA information matches the address information stored in the address table for a particular port, the switching device 12 forwards the frame to that port (the expansion bus is considered to be a port).

In addition, when the switching device 12 determines that the DA information of a received frame matches the address information stored in its address table, it asserts a match signal associated with the corresponding DA information. The match signal is supplied to other switching devices 12 in the switching unit to notify them that the corresponding DA address information is associated with the switching device 12 that originates the match signal. Thus, the other switching devices 12 in the switching unit are informed that the host with the respective DA address information is not connected to one of their own media ports. The switching device 12 only asserts the match signal on the first occasion on which it recognizes a match for the destination address of an incoming packet.

Immediately on assertion of the match signal, the switching devices 12 receiving this signal cease to flood the frame with the corresponding DA information. Also, the switching devices 12 use the received match signal to update address information in their address table. When the switching devices 12 find the respective DA information next time, they forward the corresponding frame only to the expansion bus 26 to transfer to the switching device 12 connected to the host with the respective DA information.

A switching device 12 that generates the match signal may be provided with a unique number. This would make it possible for the switching system as a whole to

forward traffic with the DA information associated with the match signal directly to the switching device 12 connected to the host with the respective DA. This could improve the efficiency of the whole switching system by allowing frames to be sent directly to this switching device, instead of having each switching device 12 send frames that do not have matching DA information to all of the other switching devices 12. Thus, the match signal sent by every switching device 12 to all other switching devices 12 in the system is unambiguously associated with the DA that causes the match signal and with the switching device that generated the match signal.

Output match pins may be provided on every switching device 12 to output the match signals. Input match pins may be provided on every switching device 12 to input the match signals. For example, as shown in Figure 1, the output match pins of the devices 12a and 12b are respectively connected to the input match pins of the devices 12b and 12c, and the output match pin of the switching device 12c is connected to the input match pin of the switching device 12a.

Alternatively, the match signal may be transferred via the expansion bus 26 as a prefix or suffix to the data frame. Such a prefix or suffix indicates that the DA information in the related data frame matches address information in one of the switching devices 12, and may uniquely identify the switching device 12 that generates the match signal.

Figure 2 is a simplified diagram illustrating one of the three switching devices 12 shown in Figure 1. The switching device 12 comprises a content addressable memory and address learning logic block 32 responsible for making decisions as to whether each frame received via either the expansion bus 26 or the media port should be forwarded, and if so, to which ports. Via an expansion bus input, the block 32 receives the SA information and DA information of frames received from the expansion bus 26. A media access control and buffer memory functions block 34 supplies the block 32 with the SA information and DA information of frames received from the network stations 14 connected to the corresponding switching device 12.

The block 32 comprises an address memory, and search logic for searching the address memory for SA and DA information retrieved from received frames. If the block 32 finds no match between the SA information of a received frame and the address information in its address memory, it adds a new address entry to the address

memory to store the SA information and information on the port associated with the SA information.

The block 32 makes a frame forwarding decision by comparing the DA information of the received frame with the address information stored in the address memory. If the address information matching the DA information is found in the address memory, the block 32 produces a forwarding control signal to forward the received frame to the appropriate media port, or the expansion bus 26. In response to the forwarding control signal, an expansion bus forwarding logic 36 forwards the received frame to the expansion bus 26. The media access control block 34 is responsible for forwarding the frame to the appropriate media port in response to the forwarding control logic.

When the address information matching the DA information of the received frame is found in the address memory, the block 32 produces a match signal. Also, the block 32 generates a match signal when a frame forwarded via the expansion bus 26 is accompanied by a match signal asserted by another switching device 12 in the switching system.

Via the match signal output of the switching device 12, the match signal is supplied to the match signal input of the switching device connected to the match signal output. In response to the match signal, the block 32 of that switching device learns the DA information of the frame associated with the match signal. For example, a new entry may be added to the address table to store the received DA information and information on the port associated with the DA information. The switching device 12 uses the address information originated by the match signal to make forwarding decisions. As discussed above, the match signal may be transferred via separate input and output match pins or via the expansion bus 26.

Thus, the match signals are used to share address table information among multiple switching devices. This concept is applicable to many different types of expansion buses. For example, Figure 3 shows another embodiment of the present invention, wherein the switch unit includes multiple switching devices 120 connected to a high bandwidth shared access expansion bus 260.

Each switching device 120 has multiple media ports that support data packet transmission and reception to and from multiple network stations. The match signals may be transferred via a separate match bus 280 or via the expansion bus 260. The expansion bus 260 and the match bus 280 may be connected to an expansion port configured for connection to any number of other similar switching units.

Thus, various types of expansion buses may be used in the switching system of the present invention. The physical implementation of the match signal depends on the characteristics of the expansion bus. If the expansion bus is a high-speed multi-master bus via which each frame is transmitted in whole, the match signal may be asserted at an early stage of the corresponding frame transfer. If the switching system uses a time division multiple access (TDMA) bus, the match signal may be asserted during the appropriate time slot.

Accordingly, the match signal accompanying a received frame enables the switching system to identify the switching device connected to the network node associated with the DA information of the received frame.

While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is Claimed Is:

1. A data communication system comprising:

multiple switching devices for switching data packets, and

an expansion bus for transferring the data packets between the switching devices;

each switching device having an address processing block for comparing destination address information of a received data packet with current address information, and producing a match signal supplied to another switching device when the destination address information matches the current information.

2. The system of claim 1, wherein the match signal identifies the switching device that generates the match signal.

3. The system of claim 1, wherein the address processing block is configured for producing a forwarding control signal for forwarding the received data packet to a destination associated with the destination address information.

4. The system of claim 3, wherein the address processing block is configured for comparing source address information of the received data packet with the current address information to update the current address information in accordance with the source address information if the source address information does not match the current address information.

5. The system of claim 4, wherein the address processing block of said another switching device is responsive to the match signal for updating the current address information in accordance with the destination address information that causes the match signal.

6. The system of claim 5, wherein each switching device comprises a match pin connected to the match pin of said another switching device to transfer the match signal.

7. The system of claim 5, wherein the match signal is transferred via the expansion bus.

8. The system of claim 5, wherein the address processing block is configured for processing the source and destination address information of data packets received from the expansion bus.

9. The system of claim 8, wherein the address processing block of a switching device is further configured for processing the source and destination address information of data packets received from network stations connected to the switching device.

10. In a data switching system having multiple switching devices, a method of data switching comprising the steps of:

comparing destination address information of a received data packet with first current address information maintained by a first switching device, and

supplying a match signal to a second switching device when the destination address information matches the first current address information.

11. The method of claim 10, wherein the second switching device stores second current information updateable in response to the match signal.

12. The method of claim 11, wherein the second current information is updated in accordance with the destination address information that causes the match signal.

13. The method of claim 12, further comprising the step of comparing source address information of the received data packet with the first current information to update the first current information in accordance with the source address information if the source address information does not match the first current information.

14. The method of claim 13, further comprising the step of comparing source address information of received data packets with the second current information to update the second current information in accordance with the source address information if the source address information does not match the second current information.

15. The method of claim 14, wherein the second switching device uses the second current information for making data packet forwarding decisions.

Abstract of the Disclosure

MATCH SIGNALS IN DATA SWITCHING SYSTEMS INCLUDING MULTIPLE SWITCHING DEVICES

A novel method of data packet switching in a data packet switching system having multiple switching devices. The method includes comparing destination address information of a received data packet with current address information maintained in an address table of one of the switching devices, and supplying a match signal to other switching devices when the destination address information matches the current address information. As a result, all other switching devices in the system are informed that the host with the destination address that caused the match signal is not connected to one of their own media ports. The match signal sent to other switching devices in the system is unambiguously associated with the destination address that caused the match. Also, the match signal may uniquely identify the switching device that generates this signal. In response to the match signal, the current address information of the other switching devices in the system may be updated in accordance with the destination address information that caused the match signal to forward traffic with that destination address to the appropriate switching device.

FIGURE 1

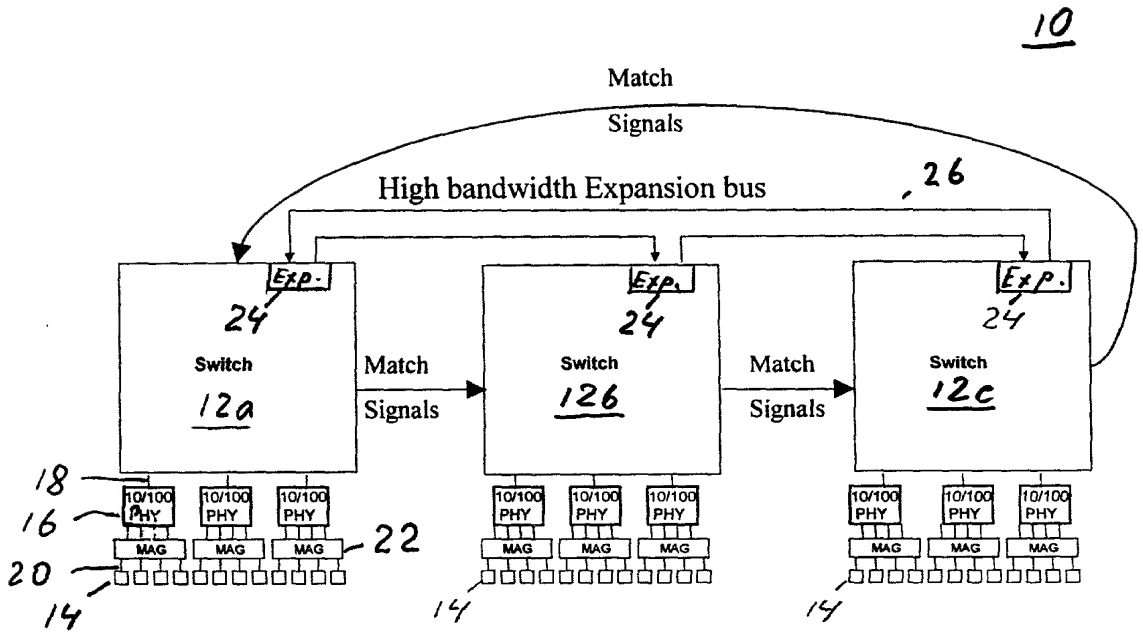

10
Match
Signals
High bandwidth Expansion bus
26
Exp.
24
Switch
12a
Match
Signals
Switch
12b
Match
Signals
Switch
12c
18
16
20
14
10/100
PHY
MAG
22

FIGURE 2

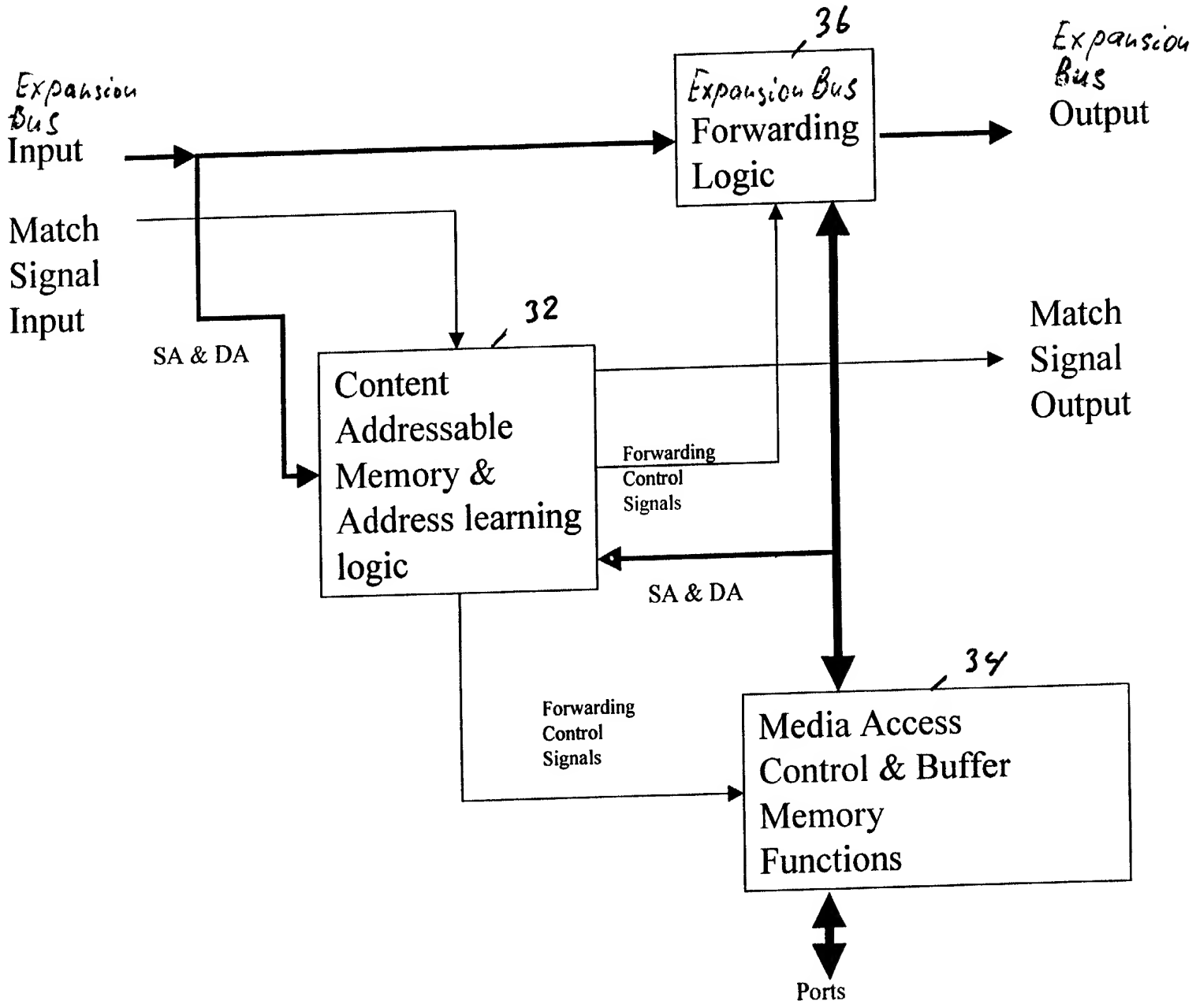
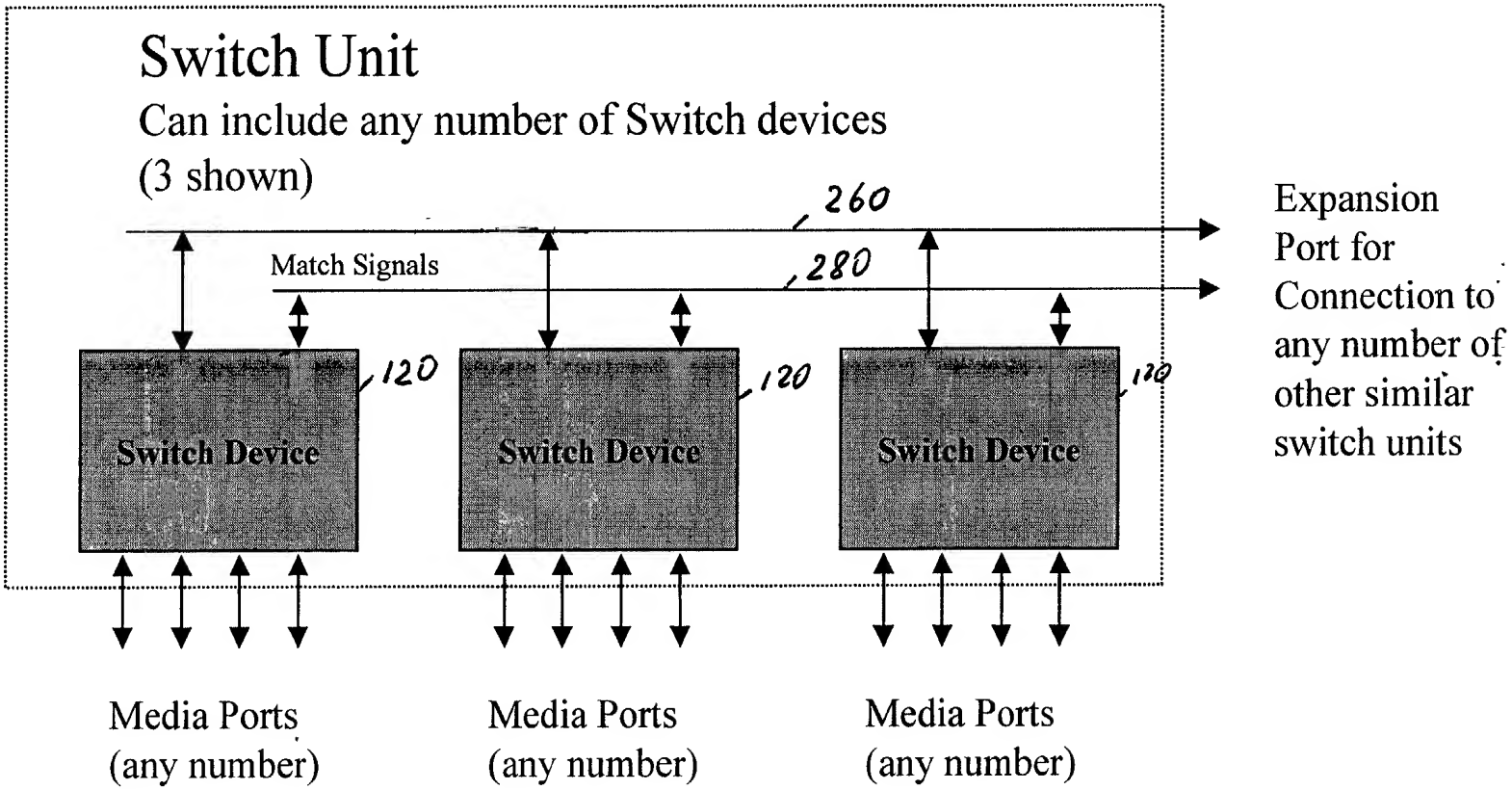

36
Expansion Bus Forwarding Logic
Expansion Bus Input
Expansion Bus Output
Match Signal Input
SA & DA
32
Content Addressable Memory & Address learning logic
Match Signal Output
Forwarding Control Signals
SA & DA
34
Forwarding Control Signals
Media Access Control & Buffer Memory Functions
Ports

FIGURE 3


Switch Unit
Can include any number of Switch devices
(3 shown)
260
Match Signals
280
120
120
120
Switch Device
Switch Device
Switch Device
Expansion Port for Connection to any number of other similar switch units
Media Ports (any number)
Media Ports (any number)
Media Ports (any number)

Docket No.: **50100-754**

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled **MATCH SIGNALS IN DATA SWITCHING SYSTEMS INCLUDING MULTIPLE SWITCHING DEVICES**, the specification of which
[x] is attached hereto [ ] was filed on as Application Serial No. and was amended on (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			**Priority Claimed**	
Number	**Country**	**Day/Month/Year filed**	**Yes**	**No**

I hereby claim the benefit under 35 USC §119(e) of any United States provisional application(s) listed below.

Prior Provisional Application(s):

Application Number	**Filing Date**

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U. S. Application(s):

Serial No.	**Filing Date**	**Status: Patented, Pending, Abandoned**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) and/or agent(s): Edward A. Becker, Reg. No. 37,777; Stephen A. Becker, Reg. No. 26,527; Marcel K. Bingham, Reg. No. 42,327; John G. Bisbikis, Reg. No. 37,095; Daniel Bucca, Reg. No. 42,368; Kenneth L. Cage, Reg. No. 26,151; Stephen C. Carlson, Reg. No. 39,929; Paul Devinsky, Reg. No. 28,553; Laura A. Donnelly, Reg. No. 38,435; Margaret M. Duncan, Reg. No. 30,879; Brian E. Ferguson, Reg. No. 36,801; Michael F. Fogarty, Reg. No. 36,139; Wilhelm F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Brian D. Hickman, Reg. No. 35,894; Eric J. Kraus, Reg. No. 36,190; Edward E. Kubasiewicz, Reg. No. 30,020; Patrick B. Law, Reg. No. 41,549; Robert E. LeBlanc, Reg. No. 17,219; Jack Q. Lever, Reg. No. 28 ,149; Raphael V. Lupo, Reg. No. 28,363; Christine F. Martin, Reg. No. 39.762; Michael E. McCabe, Jr., Reg. No. 37,182; Michael A. Messina, Reg. No. 33,424; Eugene J. Molinelli, Reg. No. 42,901; Christopher J. Palermo, Reg. No. 42,056; Joseph H. Paquin, Jr., Reg. No. 31,647; Craig L. Plastrik, Reg. No. 41,254; Robert L. Price, Reg. No. 22,685; Paul A. Roberts, Reg. No. 40,289; Gene Z. Rubinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; Michele M. Schafer, Reg. No. 34,717; David J. Serbin, Reg. No. 30,589; Glenn Snyder, Reg. No. 41,428; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Leonid D. Thenor, Reg. No. 39,397; Keith J. Townsend, Reg. No. 40,358; Leon R. Turkevich, Reg. No. 34,035; Christopher D. Ward, Reg. No. 41,367; Damian G. Wasserbauer, Reg. No. 34,749; Aaron Weisstuch, Reg. No. P41,557; Edward J. Wise, Reg. No. 34,523; Alexander V. Yampolsky, Reg. No. 36,324; and Robert W. Zelnick, Reg. No. 36,976 all of

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****

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Inventor's signature: S. McRobert Date: 6/9/2000

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